Amendments to the Specification:

Please replace paragraph **[11]** with the following amended paragraph:

In a specific alternative embodiment, the invention provides a method for processing semiconductor wafers, e.g., silicon. The method includes providing a monitor wafer, which is made of a crystalline material. The method includes introducing a plurality of particles within a depth of the material, whereupon the plurality of particles cause the crystalline material to be in an amorphous state. The method also includes introducing a plurality of dopant particles into a selected depth of the crystalline material in the amorphous state using an implantation tool. The amorphous state traps the dopant particles. The method includes subjecting the monitor wafer including the plurality of particles and dopant particles into thermal anneal process to activate the dopant. ~~The~~ A sheet resistivity is measured. The method operates the implantation tool using one or more production wafers if the dose of the dopant particles in the monitor wafer is within a tolerance of a specification limit.

Please replace paragraph **[45]** with the following amended paragraph:

[45] Figures 1 through 6 are simplified cross-sectional view diagrams illustrating a method 100 according to an embodiment of the present invention. These diagrams are merely ~~an illustration~~ illustrations, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. As shown, the method 100 begins by providing a monitor substrate 101, which can be a silicon wafer or the like. Alternative substrates can include any suitable material such as epitaxial silicon and silicon on insulator substrate. Preferably, the monitor ~~wafer~~ substrate is ~~the~~ a silicon wafer.

Please replace paragraph **[46]** with the following amended paragraph:

[46] Referring to Figure 2, the method introduces a plurality of particles 105 to cause an amorphous state within a thickness 111 of the monitor substrate. The thickness is defined to a predetermined depth 107, which can be constant or vary slightly, depending upon the application. The particles are introduced through the surface 109 of the substrate using

implantation techniques or others. As shown, the particles can be silicon bearing particles such as elemental silicon. Such silicon bearing particles can be derived from gases such as silane, dichlorosilane, any combination of these, and others. Further details of the amorphous state are described throughout the present specification and more particularly below.

Please replace paragraph **[47]** with the following amended paragraph:

[47] Next, the method introduces a dopant impurity 305 at low energy and high dose into a depth 301 of the monitor ~~wafer~~ substrate. The dopant impurity can be a boron bearing species, an arsenic bearing species, and others. The energy is often 2 KeV to less than 2 KeV, but can also be others. The dose is 4×10^{14} to 1×10^{15} atoms/cm^2, but can also be others. Preferably, the method is used for low energy high dose impurities for shallow junction devices. These devices often have junction depths of less than 40 nm, but can also be at other depths. Additionally, the shallow junction devices are often for line rules of less than 0.15 um. Of course, the particular energies, doses, and depths depend upon the application.

Please replace paragraph **[48]** with the following amended paragraph:

[48] Referring to Figure 4, ~~the~~ implanted profile 400 as a function of depth is illustrated. This profile is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many alternatives, variations, and modifications. As shown, the vertical axis 401 illustrates concentration. The horizontal axis 403 illustrates depth from the surface of the monitor substrate to the predetermined depth. The profile 405 is substantially even and then reduces in concentration as a function of depth. Further details of such profile are provided below.

Please replace paragraph **[49]** with the following amended paragraph:

[49] Figure 4A is a simplified cross-sectional view diagram of a portion of a semiconductor substrate according to an embodiment of the present invention. This ~~profile~~ diagram is merely an example, which should not unduly limit the scope of the claims herein. One of ordinary skill in the art would recognize many alternatives, variations, and modifications.

The portion 450 of the substrate includes silicon bearing species and boron bearing species. Some of the silicon bearing species ~~is~~ are from the original substrate material. Other silicon bearing species have been implanted. Such silicon bearing species have broken bonds 451 and form an amorphous state within the substrate. The substrate is substantially free from an overlying oxide layer, which may interfere with ~~the~~ boron implantation. There may be a very small layer of oxide, but is substantially ineffective as a screen oxide or other like material. Boron bearing species ~~453~~ are also included. Such boron bearing species have not been activated in part according to a specific embodiment. Accordingly, the monitor substrate including the implanted species should be subjected to a thermal process, such as rapid thermal anneal.

Please replace paragraph **[50]** with the following amended paragraph:

[50] Here, the method subjects the monitor ~~wafer~~ substrate including the plurality of particles and boron into a rapid thermal anneal process at about 700 Degrees Celsius to activate ~~the~~ boron. ~~bearing particles~~ Depending upon the embodiment, other temperatures can be used. For example, the temperature can range from about 650 Degrees Celsius to about 700 Degrees Celsius. The rapid thermal anneal process also recrystallizes certain portions of the amorphous state silicon material. The monitor ~~wafer~~ substrate is then removed and ready for subsequent processing.

Please replace paragraph **[51]** with the following amended paragraph:

[51] The method measures a sheet resistivity of the monitor ~~wafer~~ substrate. The sheet resistivity can be measured using a probe ~~and~~ tool such as KLA Tencor Rs-75, but can also be others. The sheet resistivity is kept for further analysis. The method then performs the above steps for other monitor wafers having different doses of boron impurities. The doses have also been provided with a tool that has been calibrated according to a preferred embodiment.

Please replace paragraph **[54]** with the following amended paragraph:

[54] In a specific embodiment, the invention also provides a method for manufacturing an integrated circuit device using an implantation process according to an embodiment of the

present invention. Here, the method can be used to check the process of a specific implantation tool. The method is often performed during a predetermined frequency or other desirable times for the specific implantation tool. As shown in Figure 6, the method begins at start, step 601. The method is performed for checking a specific implantation tool, step 603. Before production operation, ~~the~~ a monitor ~~water~~ wafer is (step 605) inserted into the specific implantation tool, which would be evaluated.

Please replace paragraph **[55]** with the following amended paragraph:

[55] The method ~~introduce~~ introduces a plurality of particles (e.g., silicon) within a depth of ~~the~~ a silicon material to cause an amorphous state within the silicon material. The method then ~~introduce~~ introduces boron at a selected low energy and a selected high dose into a depth of the monitor wafer. The dopant impurity can be a boron bearing species, an arsenic bearing species, and others. The selected low energy is often 2 KeV to less than 2 KeV, but can also be at others. The selected high dose is 4×10^{14} to 1×10^{15} atoms/cm^2, but can also be others. Preferably, the method is used for low energy high dose impurities for shallow junction devices. These devices often have junction depths of less than 40 nm, but can also be at other depths. Additionally, the shallow junction devices are often for line rules of less than 0.15 um. Preferably, the dose and the energy are pre-selected but are provided for process checking before ~~the~~ a production run of wafers. Of course, the particular energies, doses, and depths depend upon the application.

Please replace paragraph **[57]** with the following amended paragraph:

[57] The method measures a sheet resistivity of the monitor wafer. The sheet resistivity can be measured using a probe ~~and~~ tool such as KLA Tencor Rs-75, but can also be others. The method then determines (step 607) a dose of impurity based upon plot, which ~~had~~ has been previously explained. The method determines (step 608) ~~of~~ if the dose is within a predetermined tolerance limit for ~~the~~ an implantation process. The predetermined tolerance is often ~~the~~ a specification limit for the particular implantation ~~tool and~~ process. If ~~the~~ a tool is in specification, the method releases the tool to run production waters, step 609. Alternatively, the method turns the tool over to a maintenance and/or calibration process, step 613. Preferably, the

method runs production for at least 24 hours until another monitor water is checked to ensure the quality of the process. The method stops at step 611.

Please replace paragraph **[61]** with the following amended paragraph:

[61] We performed these experiments using conventional tools and a desire to discover improved processes for semiconductor integrated circuits. ~~continued~~ Continued device scaling often ~~required~~ requires a formation of ever-shallower, low-resistance junctions. The use of ultra-low energy implant and spike anneals ~~made~~ make it possible to develop sub-micron technology. A combination of ultra-low energy implant and spike anneals are often desirable to form ultra shallow junctions. The implantation energy can be lowered to sub KeV level. It is often necessary to monitor low energy implantation performance. Annealing is a big issue for low energy implantation monitor, out-diffusion happens when annealing without O2 or screen oxide, resulting in ~~worse uniformity~~ non-uniformity; annealing with O2 or screen oxide will often impact dosage measurement accuracy. Here, silicon implantation was used to ~~get~~ form amorphous silicon before boron implantation. The wafer can be annealed at a lower temperature without O2 or screen oxide.

Please replace paragraph **[63]** with the following amended paragraph:

We have provided our results in Table 1 of Figure 9, which shows the effect of silicon implantation on boron activation. Here, implantation conditions included silicon/20KeV/1 x 10^{15} atoms/cm^2 before boron/2KeV/4 x 10^{14} atoms/cm^2 and annealing conditions were 700°C, 30 seconds, N2 as annealing ambient. As shown in Table 1, implantation with boron only ~~shows~~ showed very high sheet resistance. Boron implanted into the wafer was not activated. Silicon implantation before Boron implantation can be helpful for boron activation, an Rs of 442.7 ohms/cm^2 was obtained (uniformity: 0.33%).

Please replace paragraph **[64]** with the following amended paragraph:

[64] As has been demonstrated, a step of silicon implant to cause amorphous silicon in a pre-determined depth before boron implant can aid in boron activation. ~~pre-amorphous of silicon implantation can be benefit for Boron activation~~. No oxygen or screen oxide was needed for annealing, ~~that will be~~ ~~good~~ which improves accuracy in ~~to~~ ~~monitor~~ monitoring low energy implanter. ~~The~~ A sensitivity of 0.83% ($\triangle$Rs/$\triangle$Dose) was obtained in the present study. Of course, one of ordinary skill the art would recognize many variations, alternatives, and modifications.